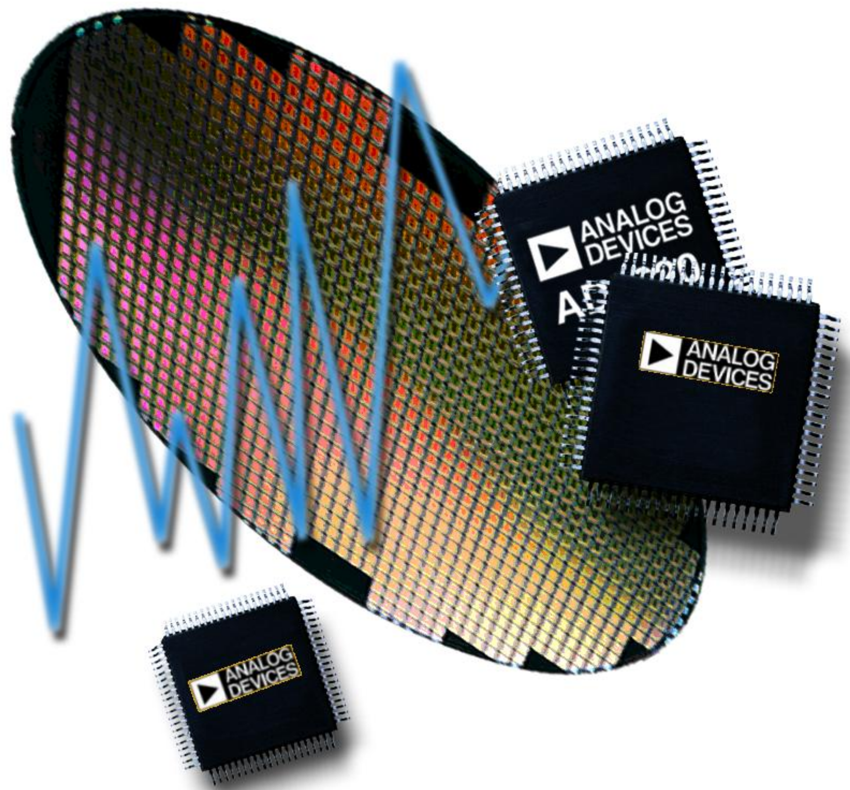
ANALOG DEVICES



Reliability Report

Report Title: SSM2166 Die Revision

Report Number: 6956

Date: 5 May 2008

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Summary

This report documents the successful completion of the reliability qualification requirements for release of the SSM2166 product in a 14-SOICnb package. The SSM2166 is a microphone preamplifier with variable compression and noise gating.

The die revision is due to the product being re-designed on a newer 8-inch bipolar process(HVBP2) at ADI-Limerick. The original design was on a 4-inch bipolar process (ECL-DLM) at ADI-Santa Clara.

Table 1: SSM2166 Product Characteristics

Device

Device / Die ID	2523ya
Die Size (mm)	1.98 x 1.58
Wafer Fabrication Site	ADI-Limerick
Wafer Fabrication Process	2um HVBP2, DP, DM
Transistor Count	194
Passivation Layer	undoped-oxide/OxyNitride
Bond Pad Metal Composition	AlCu

Package/Assembly

Available Package(s)	14-SOICnb
Body Size (mm)	4.00 x 8.75 x 1.50
Assembly Location	Carsem-S
Die Attach	Ablestik 84-1LMIS R4
Lead Frame Material	Copper
Bond Wire Type	Gold Tanaka M3
Bond Wire Dia. (mils)	1.00
Mold Compound	Sumitomo 6600H
Lead Finish	Tin Plate
Die Overcoat	Dow 4939
Moisture Sensitivity Level	1
Maximum Peak Reflow (°C)	260

Description/Results of Tests Performed

Table 2 and 3 provide a description of the qualification tests conducted and the associated test results on the SSM2166 described in the product characteristics table on the same technologies as described in the product characteristics table.

Table 2: 8-SOICnb Package Qualification Test Results

Test Name	Conditions	Specification	Device	Lot Num	Sample Size	Qty. Rejects
Autoclave [1]	121C 100%RH 2atm 168hrs	JEDEC-STD-22, Method A102	AD8023	EQM020205B	77	0
				EQM020205C	77	0
			AD71001	AB83614.1	77	0
				AB83616.1	77	0
			ADA4861-3	Q5616.4	77	0
HAST [1]	130C 85%RH 2atm, Biased 96hrs	JEDEC-STD-22, Method A110	AD71001	AB83619.1	77	0
				AB83617.1	77	0
				AB83618.1	77	0
			SSM2166	Q6956.5	30	0
Temp Cycle [1]	-65C/+150C 500cycles	JEDEC-STD-22, Method A104	AD8023	EQM020205B	77	0
				EQM020205C	77	0
			ADA4861-3	Q5616.5	77	0
Thermal Shock [1]	-65C/+150C 500cycles	JEDEC-STD-22, Method A106	ADA4861-3	Q5616.6	77	0

[1] These Samples were subjected to preconditioning (per J-STD-020 Level 1) prior to the start of the stress test. Level 1 preconditioning consists of the following:

- Bake: 24 hrs @ 125°C
- Unbiased Soak: 168 hrs @ 85°C, 85%RH
- Reflow: 3 passes through an oven with a peak temperature of 260+0/-5°C

Table 3: Process Qualification Test Results

Test Name	Conditions	Specification	Part Number	Lot Number	Sample Size	Qty. Rejects
ELF	125C 48hrs	MIL-STD-883, Method 1015	AD8675	f159516.3	630	0
				f159575.12	416	0
				f159575.3	209	0
				F159642.3	628	0
				f159654.10	59	0
				f159916.2	700	0
				f159928.2/6	700	0
				f160129.5/6	669	0
				AA13504.1	660	0
			ADR127	AA43211.1	500	0
				AA43212.1	499	0

				AA45565.1	165	0
				AA45566.1	165	0
				AA71229.1	170	0
				AA71229.2	447	0
				AA71229.3	53	0
			AD8677	AA20920.1	564	0
				AA20920.2	101	0
				AA20921.1	564	0
				AA20921.2	101	0
				R88467.1	610	0
HAST	130C 85%RH 2atm, Biased 96hrs	JEDEC-STD-22, Method A110	AD8675	f159516.6	77	0
				f159575.6	77	0
				F159642.6	77	0
			ADR127	AA40334.1	77	0
				AA40335.1	77	0
				AA71758.1	77	0
			AD8677	AA20708.1	77	0
				AA20709.1	77	0
				AA20710.1	77	0
HTOL	125C<Tj<135C, Biased 1000hrs	JESD22-A108	AD8675	AA13505.1	77	0
				f159516.9	45	0
				f159575.9	76	0
				F159642.5	77	0
			ADR127	AA37664.1	75	0
				AA37665.1	77	0
				AA71230.1	74	0
				F160129.8	77	0
				f160129.9	77	0
				f160129.4	77	0
				f159928.4	100	0
			AD8677	AA20918.1	77	0
				AA20919.1	77	0
				R88468.1	77	0

ESD Testing

The results of Human Body Model (HBM) and Field Induced Charge Device Model (FICDM) ESD testing are summarized in Table 4.

ADI measures ESD results using stringent test procedures based on the specifications listed in the below table. Any comparison with another supplier's results should ensure that the same ESD test procedures have been used. For further details, please see the EOS/ESD chapter of the ADI Reliability Handbook at http://www.analog.com/corporate/quality/manuals/.

Table 4: SSM2166 ESD Test Results

ESD Model	Package	ESD Test Spec	RC Network	Highest Pass Level	First Fail Level	Class
FICDM	8-SOICnb	ESD Assoc. STM5.3.1-1999	1Ω, Cpkg	1500V	NA	C6
HBM	8-SOICnb	ESD Assoc. STM5.1-2001	1.5kΩ, 100pF	4000V	NA	3A

Latch-up Testing

Six samples of the SSM2166 passed Latch-up testing at Ta=25°C per JEDEC Standard JESD78, Class I, Level A.

Approvals

Reliability Engineer: Robert Yhap
This report has been approved by electronic means (3.5).

Additional Information

Data sheets and other additional information are available on Analog Devices' web site at the addresses shown below.

Home Page: http://www.analog.com
Sales Info: http://www.analog.com/world/corp_fin/sales_directory/distrib.html
Reliability Data: http://www.analog.com/world/quality/read/1stpage.html
Reliability Handbook: http://www.analog.com/corporate/quality/manuals/